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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,799	08/19/2002	Weng-Hsing Huang	9222-US-PA	4097

31561 7590 01/13/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
HA, NATHAN W	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 01/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,799	HUANG ET AL.	
	Examiner	Art Unit	
	Nathan W. Ha	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

P riod for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/24/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Sogawa et al., US 5,670,402, previously cited.

Re claim 1, Sogawa et al. disclose in Figures 3 and 4, a memory device, comprising substrate (20); gate oxide layer (30), disposed on a surface of the substrate; gate disposed on a portion of the gate oxide layer; buried drain line (36), located in the substrate beside both sides of the gate; spacer (38) disposed on sidewalk of the gate; deep doped region (40) located in the substrate below a part of the buried drain line, wherein the buried drain line and the deep doped region together form a bit line of the memory device; an insulation layer (24), disposed on the gate oxide layer and above the bit line (e.g. column 6, lines 1-2); and a word line (28), disposed on the gate and the insulation layer, perpendicular to a direction of the bit line.

Re claim 2, in the memory device disclosed by Sogawa et al. the insulation layer is formed from silicon oxide (e.g. column 6, line 27).

Re claim 3, in the memory device disclosed by Sogawa et al. the spacer (38) is formed from silicon oxide (e.g. column 6, line 15).

Re claim 4, the memory device disclosed by Sogawa et al. the word line (28) is formed from polysilicon (e.g. column 6, line 55). Re claim 5, in the memory device disclosed by Sogawa et al. the deep-doped region (40) is located in the substrate beside both sides of the spacer.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 6-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu, 6,146,949 in view of Sogawa et al., US 5670,402, previously cited.

Re claim 6, Wu discloses a fabrication method for a memory device, comprising: forming a gate oxide layer (4) on a substrate (2); forming a bar-shaped conductive structure (6) on the gate oxide layer, wherein a cap layer (8) is formed on a top of the bar-shaped conductive structure; forming a buried drain line (14) in the substrate beside both sides of the bar-shaped conductive structure; forming a spacer (12) on sidewalls of the bar-shaped conductive structure and the cap layer after forming the buried drain line; and forming an insulation layer (16) above the bit line; removing the cap layer (e.g, Figure 7); forming a conductive layer on the substrate and patterning the conductive layer and the bar-shaped conductive structure in a direction perpendicular to a direction of the bit line to form a word line (18) and a plurality of gates (e.g. column 4, lines 55-

59). Wu does not disclose forming a deep doped region in the substrate beside both sides of the spacer, wherein the buried drain line and the deep doped region together form a bit line of the memory device. Sogawa et al. disclose a fabrication method for a memory device comprising forming a deep-doped region (40) in the substrate below a part of the buried drain line (36). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method disclosed by Wu to include the step of forming a deep doped region in the substrate below a part of the buried drain line as disclosed by Sogawa in order to increase reading speed of data (e.g. column 2, lines 15-18).

Re claim 7, in the modified method disclosed by Wu, there is an etching selectivity between the cap layer (8) and the spacer (12).

Re claim 8, in the modified method disclosed by Wu, there is an etching selectivity between the cap layer (8) and the insulation layer (16).

Re claim 9, in the modified method of Wu the cap layer is from silicon nitride (e.g. column 4, line 3).

Re claim 10, in the modified method of Wu, the spacer is formed from silicon oxide (e.g. column 4, line 22).

Re claim 11, in the modified method of Wu the insulation layer disclosed by Sogawa et al. is formed form silicon oxide (i.e. column 10, line 22).

Re claim 12, in the modified method of Wu, forming of the buried drain line (14) includes performing an ion implantation process using the cap layer and the bar-shaped conductive structure as an implantation mask (e.g. Figure 5).

Re claim 13, in the modified method of Wu, the deep-doped region (40) disclosed by Sogawa et al. is formed by performing an ion implantation process using the cap layer and the spacer as an implantation mask (e.g. Figure 4c).

Re claim 14, in the modified method of Wu forming of the insulation layer above the bit line comprises: forming globally an insulation material on the substrate, the insulation layer covers the cap layer; and removing a portion of the insulation material until the cap layer is exposed (e.g. column 4, lies 34-50).

Re claim 15, in the modified method of Wu, removing the portion of the insulation material includes performing back etching or chemical mechanical polishing (e.g. column 4, lies 34-50).

Re claim 16, in the modified method of Wu, forming of the bar-shaped conductive structure and the cap layer comprises: forming sequentially a conductive layer and a material (cap) layer on the gate oxide layer; and patterning the material layer and the conductive layer to form the bar-shaped conductive structure and the cap layer (e.g. Figures 2 and 3)

Re claim 17, in the modified method of Wu, forming the spacer comprises: forming a conformal silicon layer on the substrate and back-etching the conformal silicon oxide layer to form the spacer (e.g. column 4, lines 22-27).

Response to Arguments

5. Applicant's arguments filed 11/24/03 have been fully considered but they are not persuasive. For instance, Applicants submit that cited art, Sogawa, fails to disclose the

Re claim 13, in the modified method of Wu, the deep-doped region (40) disclosed by Sogawa et al. is formed by performing an ion implantation process using the cap layer and the spacer as an implantation mask (e.g. Figure 4c).

Re claim 14, in the modified method of Wu forming of the insulation layer above the bit line comprises: forming globally an insulation material on the substrate, the insulation layer covers the cap layer; and removing a portion of the insulation material until the cap layer is exposed (e.g. column 4, lies 34-50).

Re claim 15, in the modified method of Wu, removing the portion of the insulation material includes performing back etching or chemical mechanical polishing (e.g. column 4, lies 34-50).

Re claim 16, in the modified method of Wu, forming of the bar-shaped conductive structure and the cap layer comprises: forming sequentially a conductive layer and a material (cap) layer on the gate oxide layer; and patterning the material layer and the conductive layer to form the bar-shaped conductive structure and the cap layer (e.g. Figures 2 and 3)

Re claim 17, in the modified method of Wu, forming the spacer comprises: forming a conformal silicon layer on the substrate and back-etching the conformal silicon oxide layer to form the spacer (e.g. column 4, lines 22-27).

Response to Arguments

5. Applicant's arguments filed 11/24/03 have been fully considered but they are not persuasive. For instance, Applicants submit that cited art, Sogawa, fails to disclose the

gate structure as claimed in claim 1, for example, the spacer on the sidewalls of the gate and the word line on the gate. As mentioned above fig. 4c shows sidewalls 38 on the side of the gate 32. Furthermore, the combination of Sagawa and Wu indeed discloses word line 18 on the gate.

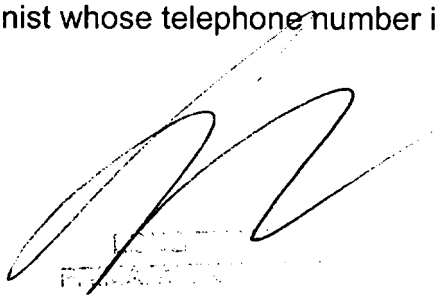
Applicants further submit that Wu fails to disclose a deep-doped region in the substrate on the both sides of the spacers. This limitation can be found in Sogawa's fig.3, for example, region 40.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan W. Ha whose telephone number is (571) 272-1707. The examiner can normally be reached on M-TH 8:00-7:00(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



Nathan Ha
January 11, 2004